REMARKS/ARGUMENTS

Claims 1-5, 9, and 10 remain pending in the present application.

Applicant appreciates Examiner's acknowledgment of allowable subject matter in claims 3-5, and 8-13.

Claim 10 is rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Claims 1-4, and 9 are rejected under 35 U.S.C. §102(b) as being anticiptated by Pao et al. (USP 4,344,081 hereinafter "*Pao*")

Claims 5 and 10 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Pao* in view of Harmel et al. (US 5,410,177, hereinafter "*Harmel*")

Claims 2, 5, and 10 have been amended in response to Examiner's objections.

The §112 Rejection

Claim 10 has been amended in response to the rejection. The feature of the "channel stopper further reduces said second breakdown voltage relative to said first breakdown voltage," has been deleted. Applicant requests that the 112 rejection be withdrawn.

The §102 Rejections

Applicant respectfully traverses the Examiner's rejection and requests reconsideration.

Applicant's Invention

Applicant's "invention relates to a semiconductor arrangement with a protection diode for improved ruggedness of a radio frequency power transistor and a self-defining method to manufacture such protection diode . . . It is an object of the present invention to provide a bipolar device comprising a RF power transistor and a protection diode and a method to manufacture such a bipolar transistor in a double poly-SI process. (Specification, page 1, lines 1-5, lines 25-

27)" "Moreover, the present invention relates to the arrangement as described . . .wherein, said first diffusion regions is a base of a bipolar transistor and said first buried layer is a collector of said bipolar transistor. Also the present invention relates . . .wherein said second diffusion region is an anode of a protection diode and said second buried layer is a cathode of said protection diode. Furthermore, the present invention relates . . .wherein said first buried layer is connected to said second buried layer, and said first and second buried layers are manufactured in the same step. (Specification, page2, lines 15-20)". Furthermore, there is a particular feature in that "simultaneously with the transistor (2), the protection diode (9) is formed."

Pao

Unlike Applicant's invention, *Pao* "relates generally to DMOS type semiconductor devices and fabrication methods therefore. This disclosure relates to an improved DMOS semiconductor type device, which can function both as a DMOS (unipolar) type device and as a bipolar transistor device. The DMOS device has two separated source regions of, for example, N+ conductivity and each of these source regions is surrounded by a P- type region, thus providing a pair of channels between each N+ source region and a common N type drain region located between the P- regions. A gate electrode is disposed over both of the channels and functions to permit electrons from the N+ source regions to flow across the P- channels into the common N type drain region when a proper bias is applied to the gate region. Each of the source regions has its own electrode and a separate electrode is provided to each of the P- regions that surround each of the respective N+ source regions. Thus, the DMOS type structure can function as a DMOS device with the electrodes to the source regions serving as source electrodes and the gate electrode functioning to permit electron flow from the separated source regions to a common drain region. Alternatively, one of the electrodes to the N+ source region could function as an emitter (or a source electrode for MOS operation) electrode with the electrode to the surrounding P- region serving as a base electrode. To complete the bipolar vertical transistor, a collector electrode is provided electrically coupled to the N- region. Alternatively, the collector electrode serves as the drain electrode if the device is operated as a DMOS device

The §102 Rejections

Claims 1-4, and 9

Pao does not disclose the features of Applicant's claimed invention. Applicant builds both a bipolar transistor and a protection diode, **simultaneously**. Refer to FIGS. 3a – 3m and FIGS. 4a – 4b. For example, the first buried layer refers to the buried layer of the transistor (See FIG. 3e), the second buried layer refers to the buried layer of the diode (See FIG. 4a). Applicant respectfully asserts that the the Office Action has misinterpreted the claimed features in referring to the "first buried layer N+" as , "a left side portion of layer 12," and the "second buried layer N" as , "a right side portion of the layer 12." Rather, these two buried layers are distinct regions, one for a transistor and one for a diode.

With respect to claims 3 and 9, in examining the drawings from *Pao* and Applicant, Pao is directed to completely different technology and uses. The Office Action's discussion of Pao's FIG. 10 "inherently showing a second diffusion region (22; P type) is an anode of pn diode and the second buried layer . . (Office Action, page 4)" is not applicable; rather the inherent pn diode may be regarded as a *parasitic* diode that is built as the transistor is fabricated. Unlike Applicant's invention, this diode has not been placed by design—being simultaneously fabricated with the bipolar transistor.

§MPEP 2131 provides:

> **"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently describe in a single prior art reference."** *Verdegaal Bros. V. Union Oil Co. of California, 814 F.2d 628,631,2 USPQ2d 1051, 1053 (Fed. Cir. 1987).* **The identical invention must be shown in as complete detail as contained in the . . .claim."** *Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPq2d 1913, 1920 (Fed. Cir. 1989).* **The elements must be arranged as required by the claim**

Consequently, Applicant respectfully asserts that a prima facie showing of anticipation has not been made. Applicant requests that the §102 rejection of claims 1-4, and 9 be withdrawn.

The §103 Rejections

The Office Action concedes that the feature of "channel stopper region (42) in said second portion of said substrate layer (13); the channel stopper region (42) being of said first conductivity type, for electrically isolating said second portion of said substrate layer (13) within the substrate (6), wherein said channel stopper region (42) is arranged to extend substantially as an extended channel stopper region (47) in between said second diffusion region (45) and said second buried layer (12)," is not present.

Harmel is directed a planar semiconductor device having a heavily doped channel stopper region of the first conductivity type and at least the following components: a Zener diode having the following regions, seen from an upper surface of the device, an upper diode region of the second conductivity type, a lightly doped first upper component region, of the first conductivity type, in which the upper diode region and the channel stopper region are formed at the upper surface, and a heavily doped lower component region of the first conductivity type; and a component having a second upper component region formed with the upper diode region in the first upper component region at the upper surface and having the same conductivity type as the upper diode region, the first upper component region, the lower component region, and a third upper component region of the first conductivity type and formed in the second upper component region at the upper surface of the device. The channel stopper region is formed adjacent to the upper diode region. A semiconductor region extending between the upper diode region and the channel stopper region has at least one of a length and a specific resistance which is dimensioned, relative to a length and a specific resistance of a semiconductor region between the upper diode region and the lower component region, such that a charge carrier breakdown of the Zener diode takes place between the upper diode region and the channel stopper region.

Unlike *Harmel*, Applicant's invention expressly states "the formation of a Zener diode disadvantageously contributes to the manufacturing time and costs of the device. Moreover, the formation of a Zener diode may be prohibited in some types of power transistor device due to restrictions imposed by the technology. For example, in a double poly-Si process for bipolar

device as known in the art, formation of a Zener diode connected to a RF power transistor is not feasible. (Specification, page 1, lines 20-25)"

MPEP §2143.01 provides:

> **The mere fact that references <u>can</u> be combined or modified does not render the resultant combination obvious unless the prior are also suggests the desirability of the combination.** *In re Mills, 916 F.2d 680, 16USPQ2d 1430 (Fed. Cir 1990)*

Thus, *Harmel* has a Zener diode components in its structure. Were Harmel modified to incorporate the features of Applicant's invention, the original intent of *Harmel's* invention would be destroyed. Applicant's invention teaches away from the formation of a Zener diode.

The arguments of *Pao* discussed *supra* are applicable in discussion of the §103 rejection. Pao does not suggest or teach Applicant's claimed invention. Alone or in combination *Pao* and *Harmel* do not teach Applicant's invention.

A case for obviousness under §103 has not been made. Applicant respectfully requests that the §103 rejections be withdrawn.

<u>Conclusion</u>

Applicant believes he has addressed the Examiner's concerns. Therefore, the claims, as amended, are now allowable over the cited references. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Please charge any fees other than the issue fee and credit any overpayments to Deposit Account 14-1270.

Respectfully submitted,

Date: 12-MAR-2004

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